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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	09/903,239
Filing Date	7/11/01
First Named Inventor	Cecchi, et al.
Art Unit	2816
Examiner Name	Long T. Nguyen
Total Number of Pages in This Submission: 18	Attorney Docket Number: 18244.2

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- ☑ Fee Attached
- ☐ Amendment/Reply
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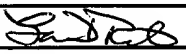
Signature	
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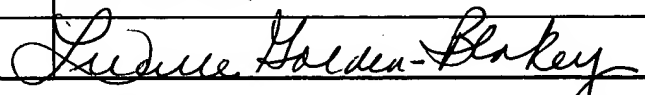
Signature		Date	7/26/04

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Cecchi, et al.** Serial No. **09/903,239** Filed: **07/11/01** For: **"CMOS Low Voltage High-Speed Differential Amplifier"**	Group Art Unit: **2816** Examiner: **NGUYEN, LONG T**

APPEAL BRIEF

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

July 23, 2004

Sir,

Pursuant to 37 C.F.R. 1.192, Applicant submits the following Appeal Brief:

REAL PARTY IN INTEREST

The real party in interest in the present application and Appeal is: International Business Machines Corporation, a corporation of New York, having a place of business at Armonk, New York 10504.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

STATUS OF CLAIMS

Claims 1-10 remain in the application and are, thus, pending. Claims 1-10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,313,696 ("Zhang") in view of U.S. Patent No. 5,039,873 ("Sasaki").

STATUS OF AMENDMENTS

No amendment has been filed since the Final Rejection of the last final Office Action.

SUMMARY OF INVENTION

In summary, the invention is a self-biasing differential amplifier that employs passive elements (such as resistors) rather than active elements (such as transistors) to bias the amplification elements. Using passive elements ensures that the amplification elements operate in saturation mode. Passive biasing elements exhibit less capacitance than the corresponding active elements and, therefore, result in a differential amplifier with a reduced response time, relative to a corresponding prior art active biasing element amplifier.

ISSUES

The following issues are presented for the Board's consideration:

1. May a rejection rely on mere functional or mechanical equivalence of two combined references without a suggestion or motivation to combine the references to support an obviousness rejection?
2. When a single figure in a single reference disclosing a microwave switch shows a symbol for a field effect transistor, an equal sign and a symbol for a resistor, and when the reference does not include any text explaining an alleged equivalence between the field effect transistor and the resistor, does the figure establish that a resistor is a known equivalent to a transistor when applied to a biasing circuit of a differential amplifier, even when evidence to the contrary has been submitted?
3. When a reference asserts that a field effect transistor is equivalent to a resistor in one operating environment, is the alleged equivalence sufficient to establish functional equivalence of a transistor to a resistor in different operating environment so as to support an obviousness rejection?
4. When an asserted suggestion to combine two references is based on an assertion that one of ordinary skill recognizes an advantageous feature of an element in one of the references, but where nothing in the record shows an awareness by those of skill in the art that applying that feature to the second reference would be advantageous, is the fact that the two references *can* be combined sufficient to establish obviousness?

GROUPING OF CLAIMS

Applicant makes no assertion regarding grouping of the claims.

ARGUMENT

Claim Rejection Under 35 U.S.C. §103

A. SUMMARY OF ARGUMENTS.

This section summarizes Applicant's arguments, according to the format of 37 CFR § 1.192 (c)(8)(iv). A more detailed argument and citation to authority is found below.

1. The Examiner has applied an incorrect standard in relying on mere functional equivalence to support the obviousness rejection.

The present invention improves upon a differential amplifier by using passive resistors rather than transistors to bias the amplifier. The Examiner rejected the claims over the Zhang reference in view of the Sasaki reference, asserting that the Zhang reference shows an amplifier as disclosed and claimed, and that the Sasaki reference shows that a resistor is a functional equivalent an always on transistor. However, the Examiner has merely asserted that if one substitutes a resistor for the biasing transistor in the Zhang reference, then the desirable result of the present invention will be achieved. This is a hindsight reconstruction of the invention that relies on mere functional equivalence and is, therefore, impermissible to support an obviousness rejection under 35 U.S.C. § 103.

2. The Examiner's assertion that a resistor is a functional equivalent to a transistor is incorrect.

The Examiner relies on the assertion that the Sasaki reference demonstrates that a resistor is a functional equivalent to an always-on transistor. However, the Sasaki reference shows an alleged equivalence only in the context of a relatively static signal redirecting circuit, not in the context of a highly dynamic amplifier circuit. Applicant has demonstrated that a resistor and a transistor behave differently from each other when used as biasing elements in a differential

amplifier. Therefore, they are not functionally equivalent and, therefore, it would not have been obvious at the time the invention was made to substitute a resistor for a transistor as a biasing element in a differential amplifier.

3. The mere fact that references *can* be combined is not sufficient to establish that it would have been obvious to combine the references.

The Examiner has asserted only that one *could* combine the Zhang reference with the asserted equivalent resistor in the Zhang reference to achieve the desirable features of the invention. Nothing in the record shows, beyond merely conclusory statements in the Office Actions, that it was generally known to substitute a resistor for a biasing transistor in an amplifier or that there is a teaching, suggestion or motivation to combine the references. Therefore, it is improper to combine Sasaki with Zhang to achieve the claimed invention to sustain an obviousness rejection.

B. DETAILED ARGUMENTS AND CITATIONS TO AUTHORITY.

1. The rejection applies an incorrect standard in relying on mere functional or mechanical equivalence to support an obviousness rejection.

In rejecting the claims, the Examiner asserted that the Zhang reference shows the invention as claimed except that it uses transistors, rather than resistors, to bias the amplifier. [3/25/04 Office Action, pp. 2-7] To support the rejection, the Examiner relied on an assertion that Sasaki shows functional equivalence between an always-on transistor and a resistor to support the rejection. [3/25/04 Office Action, p. 9]. The Examiner has not made any showing of any suggestion or motivation to combine the Zhang reference with the Sasaki reference, but stated that the existence desirable properties of the components of the invention to support the assertion of suggestion or motivation to combine references. Thus, the Examiner relies exclusively on an asserted functional equivalence of a passive resistor and an always-on transistor to support the obviousness rejection and makes no showing of a suggestion or motivation to combine the Zhang and Sasaki references to achieve the claimed invention. This is an incorrect standard and may <u>not</u> be used to sustain an obviousness rejection.

"In order to rely on equivalence as a rationale supporting an obviousness rejection, the equivalency ... cannot be based on ... the mere fact that the components at issue are functional or mechanical equivalents." MPEP § 2144.06, *see also, In re Scott*, 323 F.2d 1016 (CCPA 1963). "It is impermissible to use the claimed invention as an instruction manual or 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious." *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992), *see also* MPEP § 2143.01.

In the first Office Action (mailed August 28, 2002), the Examiner asserted that the basis for combining the teaching of Zhang with Sasaki was that "it would have been obvious to one having an ordinary skill in the art ... to substitute a resistor for each of the transistors 32, 33, 36 and 37 in Figure 2 of Zhang *because they are functionally equivalent.*" [1st Office Action, p. 4] (emphasis added). In Applicant's "Amendment and Response to First Office Action" (dated January 8, 2003), Applicant traversed the rejection. [1/8/2003 Response, p. 5]. In the Second Office Action (mailed April 21, 2003), the Examiner responded, once again, by asserting that "it is obvious to one having an ordinary skill in the art ... to replace each of the transistors 32, 33, 36 and 37 with a resistor *because they are functionally equivalent.*" [2nd Office Action, p. 8] (Emphasis added).

While the Examiner states that there is a functional equivalence between the combination of Zhang and Sasaki, as in *In re Fritch*, 972 F.2d at 1266, the Examiner relied upon hindsight to arrive at the determination of obviousness. Nothing in any of the cited art points to a suggestion to replace the biasing transistors in the circuit disclosed in the Zhang reference with a resistor. In fact, the Sasaki reference cited by the Examiner does not even show a resistor taking the place of a transistor, it merely shows that a transistor in a microwave control switch may behave like a resistor under limited circumstances. Just as in Zhang, Sasaki shows a transistor being used in its circuit as well. Sasaki simply does not show a transistor being replaced by a resistor and, therefore, drawing the conclusion that asserted Sasaki equivalence would render it obvious to replace the transistors in the Zhang circuit makes no sense.

There is nothing in either the Sasaki reference or the Zhang reference that would in any way hint at the desirability of using a resistor to bias a differential amplifier. No statement in either reference indicates that a differential amplifier (or any circuit for that matter) would work better if a resistor were to be used as a biasing element. In fact, no statement in either reference

even hints that an amplifier would work better if the biasing elements were more linear. The Examiner has merely recognized, in hindsight, that the result of the present invention is desirable and that one of skill in the art would recognize that desirability. Even assuming, *arguendo*, that a resistor is a functional equivalent to a FET[1], the assertion that they are equivalent is simply not enough to sustain an obviousness rejection under MPEP §§ 2143.01, 2144.06. For this reason, Applicant believes that the Examiner was in error and that the claims should be allowed.

2. In the operating environment of the claimed amplifier, a resistor is simply *not* a valid equivalent to a field effect transistor.

The Examiner in formulating the rejection, asserted that Sasaki shows that a resistor is an equivalent to an always-on field effect transistor (FET). However, the asserted equivalence shown in Sasaki only indicates that a FET in a microwave signal switching circuit behaves like a resistor under certain conditions, not that a FET may be replaced by a resistor in an amplifier (or even in the circuit disclosed in Sasaki, for that matter – it should be noted that the circuit in Sasaki uses only FETs, not resistors). Contrary to the assertions in the Final Office Action, a resistor is not a functional equivalent to a FET used in a differential amplifier. Applicant has argued that a resistor is not a valid equivalent to a field effect transistor in the operating environment of a differential amplifier and has presented evidence in support of the asserted non-equivalence (cites to the evidence are given below). However, the Examiner has not presented any evidence that would controvert any of Applicant's assertions in this regard.

The fundamental premise of the rejection was that FIG. 4(c) of Sasaki indicates that a resistor is equivalent to a field effect transistor in the "on" state. However, this fundamental premise is incorrect. Sasaki does not teach that a resistor is a functional equivalent to an always-on FET, but only that an always-on FET can be modeled as a resistor under certain conditions. In the environment of the amplifier disclosed in Zhang, a transistor would *not* act in the same way that a passive resistor would. Thus, as will be shown below, the equivalence model shown in FIG. 4(c) of Sasaki is *not* a correct model for differential amplifiers. Therefore, one of ordinary skill would *not* have recognized a resistor to be an equivalent to a transistor as a biasing element in a differential amplifier, as claimed in the present application.

A. Technical Background

[1] Which Applicant disputes.

As is generally known to those of skill in the electrical arts, the resistance of a resistor is constant over the normal operating range of voltages applied to the resistor. According to Ohm's law, the voltage (V_R) across a passive resistor is proportional to the resistance (R) of the resistor times the current (I_R) flowing through the resistor. Thus, one can determine the resistance of the resistor according to the following formula: $R = V_R \div I_R$. Given the constant resistance of a resistor, the current flowing through a resistor will always be directly and inversely proportional to the voltage. Thus, a curve relating resistor current (I_R) to resistor voltage (V_R) for a resistor starts at the origin of the current-voltage curve and is a straight line for all of the normal operating range of the ideal resistor. The resistance is equal to the slope of the line and a curve of the resistance (R) of a resistor is always a flat horizontal line (as shown in Exhibit A of the 12/15/03 Response).

A resistance curve for a FET is different. The current (I_D) flowing through the drain of a FET is a non-linear function of the drain-to-source voltage (V_{DS}) and the gate-to-source voltage (V_{GS}) of the FET. This functional relationship is shown graphically in Exhibit B, p. 313, Fig. 8.15. Exhibit B of the 12/15/03 Response is a relevant excerpt taken from Sedra and Smith: Micro-Electronic Circuits (which is one of the most highly used texts used to teach upper-level microelectronic circuit analysis courses in the electrical engineering curricula of major universities throughout the world). Exhibit B shows that in a FET, a plot of I_D versus V_{DS} gives rise to a plurality of curves, one for each value of V_{GS}.

As demonstrated in Exhibit C of the 12/15/03 Response (which is a graphic demonstration of a resistance versus gate voltage curve), if V_G is held constant in the always "on" state (as in the biasing transistors of Zhang) and the source is allowed to vary, then the value of V_{GS} will also vary between a maximum level when V_S is at a minimum to a minimum level when V_S is at a maximum. V_{DS} will vary in a corresponding manner. As V_{GS} varies, the I_D-V_{DS} curve for the transistor will change in a non-linear manner as different I_D-V_{DS} curves (each reflecting a different value of V_{GS}) are applied. Thus, the resistance of the transistor will also vary. Therefore, if the source voltage of a transistor varies and the gate voltage is held constant, then the transistor is not correctly modeled as a resistor, which has a horizontally flat resistance model.

The equivalence model of Sasaki is merely an approximation that is valid only when V_{GS} is held constant and V_{DS} is allowed to vary only slightly or not at all. In such a situation, the

resistance remains approximately constant and resembles the resistance curve of a resistor. On the other hand if the source voltage V_S varies (as in the case of a differential amplifier), then the I_D versus V_{DS} curve changes in a dramatically non-straight line manner and, thus, the resistance of the FET varies in a clearly non-linear manner. Therefore, if the operating environment of a FET with a gate tied to a voltage includes a source voltage that varies over any appreciable range, then the FET will exhibit a varying resistance and is not properly modeled as a passive resistor. This is the case when the FET is used in a differential amplifier.

B. Application to Rejection

The FET-resistor equivalence model shown in FIG. 4(c) of Sasaki is valid *only* when a FET is operating with a gate-to-source voltage (V_{GS}) that is held substantially constant, and then it is a useful model *only* so long as the drain-to-source voltage (V_{DS}) is maintained within a narrow range. However, as will be demonstrated below, the biasing FETs employed in Zhang have widely varying source voltages and, thus, widely varying V_{GS}. Therefore, a resistor is not a functional equivalent of a FET when used as a biasing transistor in a differential amplifier.

It is important to remember that the Sasaki model is presented in the context of a microwave switched line phase shifter. [Sasaki, Col. 1, lines 5-10] The incompleteness of the Sasaki equivalence model of FIG. 4(c) may be insignificant in the context of a microwave switched line phase shifter as shown in Sasaki. This is because the approximation of FIG. 4(c) of Sasaki applies only when the FET is held in an "on" state [Sasaki, Col. 1, lines 20-22], in which a constant V_{GS} (e.g., -5V) is applied to the FET [Sasaki, Col. 1, lines 26-31]. Given that a microwave RF signal is then transmitted through the FET, one can assume that the source to drain voltage (e.g., the voltage between node 1 and node 2 in FIG. 4(a)) would be essentially constant. Otherwise, the varying resistance (and, thus, the varying impedance) resulting from a varying V_{DS} would result in distortion of the RF signal being switched by the circuit. Thus, FIG. 4(c) shows an approximate equivalence between a FET and a resistor only in the special case when the V_{GS} and V_{DS} of the FET are held at an essentially constant value. Therefore, the equivalence model shown in Sasaki, FIG. 4(c), is not a useful approximation when V_S is likely to vary.

The Examiner cited Stockstad (U.S. Patent No. 6,429,685) [Final Office Action, p. 9]. However, the Examiner's reference was incomplete. While Stockstad indeed states"[t]he impedance of a passive resistor is inherently linear," [Stockstad, col. 5, lines 19-20] the sentence

immediately preceding the cited passage refers to "the inherent non-linearity of the output impedance of a transistor," [Stockstad, col. 5, lines 18-20] Clearly, the only conclusion one can draw from the portion of Stockstad cited by the Examiner is that a resistor (which is inherently linear) and a transistor (which is inherently non-linear) are not functional equivalents. Thus, Stockstad serves only to further contrast a FET from a linear resistor and demonstrates the inadequacy of the equivalence model disclosed in Sasaki.

Unlike the circuit in Sasaki, the biasing transistors shown in FIG. 2 of Zhang (32, 33, 35 and 37) are likely to have a source voltage (V_S) that varies significantly. While the gate voltages of these transistors are tied either to V_{dd} or to Ground, the source voltages are coupled to nodes that have voltages that will vary from near ground to near V_{dd} (Col. 7, lines 12-15). Because the source voltages vary significantly and the gate voltages are held constant, V_{GS} for these transistors varies significantly during normal operation. Thus, the resistance of these transistors would also vary significantly, in contrast to the resistance of a passive resistor, as claimed. For example, as shown in Exhibit C of the 12/15/03 Response, when V_S is at its minimum (A), the values of both V_{DS} and V_{GS} both are at their maximum, and the I_D/V_{DS} curve of the FET is the top curve and the FET is operating in the saturation mode. On the other hand, as V_S goes to its maximum, the values of both V_{DS} and V_{GS} go to their minimum and the I_D/V_{DS} curve is the bottom curve. The operating point on each of these curves gives the resistance shown by the FET for the given value of V_S, which clearly varies as a function of V_S.

The analysis performed by Mr. Preuss confirms this. (A copy of the relevant curves[2] was shown in Exhibit D of the 12/15/03 Response.) In Fig. 2 of the Preuss Submission, the dotted line is a graph of the source-drain resistance of a biasing FET (Item No. 36 shown in FIG. 2 of Zhang, *see also*, ¶ 8 of the Preuss § 1.132 Affidavit) during normal operating conditions of the Zhang amplifier. The solid line is a graph of the resistance of a resistor put in place of this FET. The inputs and outputs used in this simulation are shown in FIG. 3 of Attachment C, where input INP corresponds to "ina" of Zhang and INM corresponds to "inb" of Zhang (item nos. 10 and 12 in FIG. 2, respectively). As is clearly shown in the Preuss simulation, a value in which "ina" is low and "inb" is high causes the resistance of FET 36 to be virtually 0 Ohms. When "ina" is

[2] Additional labeling has been applied to the curves shown in Exhibit E to improve clarity. Applicant hereby asserts that the curves themselves are identical to the curves submitted with the § 1.132 Affidavit filed on September 19, 2003. The original of this figure is found at submission filed 9/19/2003, Attachment C, Fig. 2

high and "inb" is low for a relatively long period of time, the resistance of FET 36 goes up to its maximum resistance. If this situation lasts for a relatively shorter period of time, the resistance never reaches its maximum resistance. In stark contrast, the resistance curve of a similarly placed passive resistor is flat throughout the simulation. This clearly shows that the relevant transistors from FIG. 2 of Zhang do not behave linearly, as do passive resistors. Therefore, a resistor (which has a flat resistance curve) is not a functional equivalent to a transistor that is used to bias an amplifier (which has a varying resistance curve). Therefore, it would not have been obvious to one of skill in the art to combine the resistor shown in Sasaki with the amplifier shown in Zhang to achieve the claimed invention.

Furthermore, the Sasaki equivalence model makes no mention of any capacitance in the FET. For the equivalence model of Sasaki to be correct, a FET in the "on" state would have a capacitance equal to that of a resistor, which is clearly not true when applied to an amplifier. A correct FET model showing capacitance is shown in Exhibit E of the 12/15/03 Response, a relevant excerpt taken from Hodges and Jackson: Analysis and Design of Digital Integrated Circuits (which is a standard text used to teach graduate level transistor analysis courses in electrical engineering at many major universities). A FET, even in the always "on" state exhibits the following capacitances: gate-to-drain; gate-to-source; gate-to-base; drain-to-base; and source-to-base. [Exhibit E of the 12/15/03 Response, Figure 2.6, p. 53 – the most complete model for a FET is shown in Figure 2.8, p. 57]. These capacitances can introduce significant cumulative time delays in a dynamic circuit (as has been shown previously in the analysis performed by Mr. Preuss [Submission filed 9/19/2003]). While the FET capacitances may be insignificant in the circuit disclosed Sasaki, they introduce important delays in a differential amplifier, as claimed in the present application. (The present application explicitly states that "resistors have approximately one tenth the capacitance of a transistor gate of similar size." [*See*, Present Application, p.5, lines 5-6]. It is the decreased capacitance of the present invention that gives rise to the improvements shown in the Preuss analysis.

Because the resistance model shown in FIG. 4(c) of Sasaki is not a valid resistance model in the operating range of a FET used in the amplifier of Zhang and because the model shown in FIG. 4(c) of Sasaki does not include the capacitances that are significant in the amplifier disclosed in Zhang, the equivalence model shown in FIG. 4(c) of Sasaki is *not* valid in the context of the amplifier shown in Zhang. Therefore, one of ordinary skill in the art would not

recognize any equivalence between a linear resistor and a biasing FET and, therefore, one of ordinary skill in the art would have no motivation to combine Zhang with Sasaki to achieve the invention claimed in the present application. For this reason, Applicant believes that the Examiner was in error and that the claims should be allowed.

3. The fact that references *can* be combined is not sufficient to establish obviousness.

None of the office actions include any indication that there is a suggestion of the desirability to combine Sasaki with Zhang. However, "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." MPEP §2143.01 (emphasis in original). "[T]o establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant." *In re Kotzab*, 217 F.3d 1365, 1369 (Fed. Cir. 2000). Before the PTO may combine the disclosures of two or more prior art references in order to establish *prima facie* obviousness, there must be some suggestion for doing so, found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. *In re Jones*, 958 F.2d 347, 351 (Fed. Cir. 1992).

Most if not all inventions arise from a combination of old elements. *See In re Rouffet,* 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457 (Fed.Cir.1998). Thus, every element of a claimed invention may often be found in the prior art. However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See id.* Rather, to establish obviousness based on a combination of the elements disclosed in the prior art, there must be some motivation, suggestion or teaching of the desirability of making the specific combination that was made by the applicant. *In re Kotzab*, 217 F.3d at 1369. In this context, "broad conclusory statements standing alone are not 'evidence.'" *Id.*

In the Office Action mailed 10/16/03, the Examiner acknowledged that to sustain an obviousness rejection, there must be "some teaching, suggestion, or motivation to [combine the references] found in either the references themselves or in the knowledge generally available to one of ordinary skill in the art." [10/16/03 Office Action, p. 9] However, he concluded the paragraph with only a statement to the effect that an always-on transistor and a resistor "are

functionally equivalent" [10/16/03 Office Action, p. 9] and noted "the advantage of using a passive resistor because the impedance of a passive resistor inherently is linear." *Id.* Thus, the Office Action made no statement about the suggestion or motivation to combine the Zhang and Sasaki references. At best, the Office Action takes notice that the asserted that the functional equivalence provides the suggestion or motivation to combine.

Pursuant to MPEP § 2144.03(C), Applicant traversed this notice as not properly based upon common knowledge and respectfully requested that the Examiner provide documentary evidence that shows a teaching, suggestion or motivation to combine the cited references. [12/15/03 Response, p. 10] In response to a challenge to produce documentary evidence of a suggestion or motivation to combine the references under MPEP § 2144.03(C), no such documentary evidence was provided. The Examiner's only response was that "the office action clearly states that the advantage of using passive resistor (*sic*) because the impedance of passive resistor inherently is linear ... and by Ohm's law V=IR, on skill (*sic*) in the art also recognizes that the passive resistor is linearly (*sic*)." The Examiner merely restated that the advantage of using a passive resistor was its linearity and that one of skill in the art recognizes its linearity, without any indication as to why that known linearity is a suggestion to combine Sasaki with Zhang. Thus, the Examiner is responding with only broad conclusory statements indicating that because the claimed invention achieved advantages, it would have been obvious to combine the cited references.

Applicant does not dispute that it is known that a passive resistor in known to be linear, and that this known linearity of a passive resistor provides one of the advantages of the present invention. Applicant asserts, however, that at it was not obvious to employ a passive resistor in a differential amplifier, thereby taking advantage of the linear property of the passive resistor.

By demonstrating functional non-equivalence with the Preuss simulation and other evidence, Applicant met its burden of showing non-obviousness under MPEP §2143.01. The Examiner then had the burden of presenting prior art that "suggests the desirability of the combination." MPEP §2143.01. Nowhere in the record is there any indication that prior art "suggests the desirability of the combination" of a passive resistor with a differential amplifier (such as the amplifier disclosed in Zhang). Therefore, the mere fact that Zhang and the equivalence model shown in Sasaki "<u>can</u> be combined or modified does not render the resultant

Appendix

1. A differential amplifier for providing common-mode rejection while providing differential-mode amplification, comprising:
   a. an active differential amplification element electrically coupled to a first input signal, a second input signal and an output signal, the active differential amplification element also electrically coupled to a first voltage and a different second voltage; and
   b. a passive bias element electrically coupled to the active differential amplification element, the passive bias element capable of biasing the active differential amplification element so that the active differential amplification element operates in a saturation mode, thereby generating the output signal so that the output signal corresponds to a voltage difference between the first input signal and the second input signal.

2. The differential amplifier of Claim 1, wherein the active differential amplification element comprises:
   a. a first transistor having a first source electrically coupled to [a] the first voltage, a first gate electrically coupled to a first node and a first drain, the first node being a bias node;
   b. a second transistor having a second drain, a second gate electrically coupled to the first node and a second source electrically coupled to [a] the second voltage different from the first voltage;
   c. a third transistor having a third source electrically coupled to the first voltage, a third drain and a third gate electrically coupled to the first node;
   d. a fourth transistor having a fourth drain, a fourth gate electrically coupled to the first node and a fourth source electrically coupled to the second voltage;
   e. a fifth transistor having a fifth source electrically coupled to the first voltage, a fifth drain electrically coupled to a second node and a fifth gate electrically coupled to the first node;

f. a sixth transistor having a sixth drain electrically coupled to a third node, a sixth gate electrically coupled to the first node and a sixth source electrically coupled to the second voltage;

g. a seventh transistor having a seventh source electrically coupled to the second node, a seventh drain electrically coupled to the second drain, and a seventh gate electrically coupled to a first input signal;

h. an eighth transistor having an eighth drain electrically coupled to the first drain, [and] an eighth source electrically coupled to the third node and an eighth gate electrically coupled to the first input signal;

i. a ninth transistor having a ninth source electrically coupled to the second node, a ninth gate electrically coupled to a second input signal and a ninth drain electrically coupled to the fourth drain; and

j. a tenth transistor having a tenth drain electrically coupled to the third drain, a tenth gate electrically coupled to the second input signal and a tenth source electrically coupled to the third node.

3. The differential amplifier of Claim 2, wherein the passive bias element comprises:

a. a first resistor electrically coupling the first drain to the first node;

b. a second resistor electrically coupling the second drain to the first node;

c. a third resistor electrically coupling the third drain to [an] the output signal; and

d. a fourth resistor electrically coupling the fourth drain to the output signal.

3. The differential amplifier of Claim 1, wherein the passive bias element comprises:

a. a first resistor electrically coupling the first drain to the first node;

b. a second resistor electrically coupling the second drain to the first node;

c. a third resistor electrically coupling the third drain to an output signal; and

d. a fourth resistor electrically coupling the fourth drain to the output signal;

4. The differential amplifier of Claim 1, wherein the first transistor, the third transistor, the fifth transistor, the seventh transistor and the ninth transistor each comprise a p-channel device.

5. The differential amplifier of Claim 1, wherein the second transistor, the fourth transistor, the sixth transistor, the eighth transistor and the tenth transistor each comprise an n-channel device.

6. The differential amplifier of Claim 1, wherein the second voltage is electrically coupled to a common ground.

7. A differential amplifier for providing common-mode rejection while providing differential-mode amplification, comprising:
   a. a first transistor having a first source electrically coupled to a first voltage, a first gate electrically coupled to a first node and a first drain, the first node being a bias node;
   b. a second transistor having a second drain, a second gate electrically coupled to the first node and a second source electrically coupled to a second voltage different from the first voltage;
   c. a first resistor electrically coupling the first drain to the first node;
   d. a second resistor electrically coupling the second drain to the first node;
   e. a third transistor having a third source electrically coupled to the first voltage, a third drain and a third gate electrically coupled to the first node;
   f. a fourth transistor having a fourth drain, a fourth gate electrically coupled to the first node and a fourth source electrically coupled to the second voltage;
   g. a third resistor electrically coupling the third drain to an output signal;
   h. a fourth resistor electrically coupling the fourth drain to the output signal;
   i. a fifth transistor having a fifth source electrically coupled to the first voltage, a fifth drain electrically coupled to a second node and a fifth gate electrically coupled to the first node;
   j. a sixth transistor having a sixth drain electrically coupled to a third node, a sixth gate electrically coupled to the first node and a sixth source electrically coupled to the second voltage;

k. a seventh transistor having a seventh source electrically coupled to the second node, a seventh drain electrically coupled to the second drain, and a seventh gate electrically coupled to a first input signal;

l. an eighth transistor having an eighth drain electrically coupled to the first drain, and an eighth source electrically coupled to the third node and an eighth gate electrically coupled to the first input signal;

m. a ninth transistor having a ninth source electrically coupled to the second node, a ninth gate electrically coupled to a second input signal and a ninth drain electrically coupled to the fourth drain; and

n. a tenth transistor having a tenth drain electrically coupled to the third drain, a tenth gate electrically coupled to the second input signal and a tenth source electrically coupled to the third node.

8. The differential amplifier of Claim 7, wherein the first transistor, the third transistor, the fifth transistor, the seventh transistor and the ninth transistor each comprise a p-channel device.

9. The differential amplifier of Claim 7, wherein the second transistor, the fourth transistor, the sixth transistor, the eighth transistor and the tenth transistor each comprise an n-channel device.

10. The differential amplifier of Claim 7, wherein the second voltage is electrically coupled to a common ground.

combination obvious." For this reason also, Applicant believes that the Examiner was in error and that the claims should be allowed.

CONCLUSION

For the reasons enumerated above, Applicant believes that the examination was in error and requests that all claims be allowed.

No addition fees are believed due. However, the Commissioner is hereby authorized to charge any additional fees which may be required, including any necessary extensions of time, which are hereby requested, to Deposit Account No. 502666.

7/23/04
Date

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being placed in the U.S. Mail and addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date written below.

Lucille Golden-Blakey

7/26/04
Date